IN THE SPECIFICATION

Please amend the paragraph on page 1 extending from line 5 to line 12, as follows:

B1

The present invention provides a capacitor for a ferroelectric memory and the like, and a process for manufacturing the same. More particularly, the present invention relates to a process for manufacturing a semiconductor device which has a capacitor comprising a lower electrode layer, a ferroelectric layer and an upper electric layer, which can suppress ~~a~~ peeling between the layers while maintaining electrical properties of the ferroelectric layer.

Please amend the paragraph on page 1 extending from line 15 to line 24, as follows:

B2

Ferroelectric memories in the ~~Recently, a ferroelectric memory has focused attention in a~~ semiconductor field have recently attracted attention. A ferroelectric memory is a next generation memory ~~in the next generation~~ which is characterized by ~~a~~ quick response, ~~a~~ random access, multiple rewriting, ~~a~~ low power consumption ~~power~~ and the like. In the current ferroelectric memory, a transistor is formed, followed by formation of a capacitor comprising an electrode and a ferroelectric layer. These steps are usual processes as described in the Example of JP-A 11-214655. An embodiment of the prior art will be explained below using Figures 5A - 5G ~~5 and 6 below~~.

Please amend the paragraph on page 2 extending from line 11 to line 24 as follows

B3

After that, a 1.5-μm thick photoresist pattern **26** for processing the upper electrode is formed on the upper electrode layer **25.** ~~and, then, the~~ The upper electrode **25** is then processed by dry etching (Figure 5B). Dry etching is performed mainly by sputter etching with Ar by highly dissociating a mixture gas of Cl_2 and Ar under a high vacuum at 3 mTorr

or less, for example, on a high density plasma etching apparatus using an Inductive Coupling Plasma (ICP) and the like. Generally, since vapor pressures of Pt and Ir are very low due to their low reactivity, Pt and Ir dissociated by sputter etching re-adhere to a sidewall of the pattern even after etching. By adding Cl_2, F_2 and the like to the etching gas, materials adhering on the sidewall are converted to chlorine or fluorine and the like so that they can be removed in the later step of washing.

Please amend the paragraph extending from page 2, line 25, to page 3, line 3, as follows:

Then, an etching ~~depot~~ deposit **27** adhering to the sidewall of the pattern is removed. ~~and, subsequently,~~ Subsequently, a remaining resist pattern is removed by using a down flow O_2 ashing apparatus and the like (Figure 5C).

Please amend the paragraph extending from page 3, line 12, to page 3, line 14, as follows:

After that, the etching ~~depot~~ deposit **29** adhering to the pattern side wall is removed by washing. ~~and, then, a~~ A remaining resist is then removed by down flow O_2 ashing and the like (Figure 5E ~~6E~~).

Please amend the paragraph extending from page 3, line 15, to page 3, line 19, as follows:

Similarly, a 2.0-μm thick photoresist pattern **30** for processing a ferroelectric layer is formed on the processed upper electrode layer **25**, the processed ferroelectric layer **24** and the lower electrode layer **23**, and the lower electrode layer **23** is processed by dry etching (Figure 5F ~~6F~~).

Please amend the paragraph extending from page 3, line 23, to page 4, line 1, as follows:

After that, the etching ~~depot~~ deposit **31** adhering to the pattern side wall is removed by washing. ~~and, then, a~~ A remaining resist is then removed by down flow O_2 ashing and the like (Figure 5G ~~6G~~).

Please amend the paragraph extending from page 4, line 11, to page 4, line 13, as follows:

However, this conventional process has a problem in that a layer-peeling phenomenon occurs between an electrode layer and a ferroelectric layer when a capacitor is formed. Fig. 6 illustrates upper electrode layer 25 peeling from ferroelectric layer 24.

Please amend the paragraph extending from page 4, line 14, to page 4, line 21, as follows:

The layer-peeling phenomenon occurs when a ~~depot~~ deposit is washed after etching each of the layers, and in a final annealing. Therefore, it can be considered that a lift-off phenomenon caused by penetration of a solution (for washing a ~~depot~~deposit) into a gap between the electrode layer and the ferroelectric layer, and interlayer separation due to a difference in a layer shrinkage rate between the electrode layer and the ferroelectric layer in annealing directly result in the layer peeling.

Please amend the paragraph extending from page 4, line 22, to page 5, line 5, as follows:

From an examination of the conventional semiconductor devices, ~~it is demonstrated~~ that peeling of the upper electrode layer tends not to occur as the surface morphology of the ferroelectric layer becomes ~~is~~ worse. On the other hand, ~~and that as the~~ with better surface

B10 end

morphology of the ferroelectric layer~~,~~ (that is, the denser film density) ~~results in the~~ better electric properties result. Therefore, it is currently difficult ~~to accomplish~~ to improve electrical properties and to decrease film peeling simultaneously, resulting in a big problem.

Please insert a new paragraph after the paragraph that currently ends at page 5, line 5, the new paragraph being as follows:

B11

It has been proposed to attempt to prevent the peeling by putting a dielectric layer with a high adherability between the electrode layer and the ferroelectric layer. Yet such proposal has definite disadvantages such as deterioration in electrical properties of the ferroelectric layer, process complication and the like. Thus, an optimal method has not yet been established.

✓ *Please delete the paragraph which extends from page 5, line 8, to page 5, line 14.*

Please amend the paragraph extending from page 5, line 20, to page 6, line 1, as follows:

B12

According to the present invention, peeling between a first layer and an upper layer formed on the first layer is prevented. Whereas heretofore peeling has been caused by penetration between the layers of a bath or a layer shrinkage in a step of heating, the surface of the first layer is uniquely formed to resist peeling. A ~~since a~~ convex or concave region is formed on a surface of a first layer by etching, ~~peeling between the first layer on which the convex or concave region has been formed and an upper layer formed on the first layer, which is caused by penetration of a bath or a layer shrinkage in a step of heating, is prevented~~ resulting in an interface between the layers configured to resist the peeling (referred to as an "anchor effect").

Please amend the paragraph extending from page 6, line 7, to page 6, line 9, as follows:

B13

Figure 2A - Figure 2K are ~~is a~~ cross-sectional ~~view~~ views illustrating ~~a step~~ steps of manufacturing a semiconductor device according to ~~of~~ an embodiment of ~~according to~~ the present invention.

Please amend the paragraph extending from page 6, line 10, to page 6, line 12, as follows:

B14

Figure 3 is a cross-sectional view illustrating ~~a step of manufacturing~~ a semiconductor device of ~~an~~ another embodiment according to the present invention.

Please amend the paragraph extending from page 6, line 13, to page 6, line 15, as follows:

B15

Figure 4 is a cross-sectional view illustrating ~~a step of manufacturing~~ a semiconductor device of ~~an~~ a further embodiment according to the present invention.

Please amend the paragraph extending from page 6, line 16, to page 6, line 18, as follows:

B16

Figure ~~5~~ 4A - Figure 4G are ~~is a~~ cross-sectional ~~view~~ views illustrating ~~a step~~ steps of manufacturing a semiconductor device according to a conventional technique.

Please delete the paragraph extending from page 6, line 19, to page 6, line 21.

Please amend the paragraph extending from page 6, line 22, to page 6, line 23, as follows:

B17

Figure 6 ~~7~~ is a schematic illustration showing film peeling which occurs in a conventional semiconductor device.

Please delete the paragraph on page 7, line 3.

Please amend the paragraph extending from page 7, line 2, to page 7, line 15, as follows:

~~First, a problem of peeling between an upper electrode and a ferroelectric layer beneath the upper electrode layer is explained.~~ After a ferroelectric layer is formed, a resist pattern is formed on a region in which the upper electrode is processed and formed. The ferroelectric layer is~~,~~ then~~,~~ etched to make a convex or concave pattern on the surface of the ferroelectric layer. The size of this pattern should be controlled so that the ~~convex~~ pattern does not lap over outside of the upper electrode pattern in the subsequent step of forming the upper electrode, taking into consideration fluctuations ~~with considering fluctuation~~ in a pattern line width, an alignment deviation and the like. That is, a line width of the resist pattern for making the ~~convex~~ pattern is made to be narrower than the minimal line width of the upper electrode by a margin for the alignment deviation.

B18

Please amend the paragraph extending from page 8, line 1, to page 8, line 9, as follows:

After etching the ferroelectric layer, a ~~depot~~ deposit and the remaining resist layer are removed by washing and ashing and, then, an upper electrode is formed by sputtering. By carrying out subsequent processes after the formation of the upper electrode, peeling can be prevented due to the anchor effect as compared with the case where the upper electrode attaches a smooth ferroelectric layer. The above-mentioned means can be applied to an interface between the lower electrode and the ferroelectric layer to obtain the anchor effect.

B19

Please amend the paragraph extending from page 8, line 14, to page 8, line 22, as follows:

A semiconductor device according to the Example of the present invention is shown in Figure 1. As shown in Figure 1, the semiconductor device of the present invention is characterized in that an upper electrode **17** and a ferroelectric layer **14** have a convex region. By this constitution, a layer peeling can be suppressed. In this Example, one convex region is formed on one layer, but a plurality of convex regions may be formed on one layer. Alternatively, a concave region may be formed in place of the convex region.

Please amend the paragraph extending from page 8, line 23, to page 8, line 25, as follows:

Figures 2A ~~– D, Figures 3E – H, and Figures 4I –~~ – 2K are schematic illustrations showing procedures for manufacturing the semiconductor device shown in Figure 1.

Please amend the paragraph extending from page 9, line 1, to page 9, line 6, as follows:

First, on a semiconductor flat substrate **11** on which a transistor is formed and which is covered with an insulation layer, an adhesion layer **12** is deposited to 50 nm, for example, by sputtering TiO_2, TiN, Al_2O_3, TaSiN and the like. These layers may also be obtained by forming a Ti, Al, TaSi layer and the like by sputtering, and oxidizing or nitridizing.

Please amend the paragraph extending from page 10, line 9, to page 10, line 15, as follows:

After etching, an etching ~~depot~~ deposit **16** adhering to the pattern sidewall is removed by washing (e.g., by dipping into 10% concentration hydrochloric acid for 30 seconds). ~~and, then, the~~ The remaining resist pattern **15** is then removed by ashing (e.g., on

B23

a microwave down flow ashing apparatus: Microwave power 1000 W; Wafer temperature 250 C; O_2 flow rate 1000 sccm; Treatment time 3 minutes) (Figure 2D).

Please amend the paragraph extending from page 10, line 16, to page 10, line 19, as follows:

B24

An upper electrode layer **17** is formed on the ferroelectric layer **14** thus fabricated by depositing, for example, Pt, Ir, IrO_3 and the like at a thickness of 100 nm by a conventional method such as sputtering (Figure 2E ~~3E~~).

Please amend the paragraph extending from page 10, line 20, to page 11, line 6, as follows:

B25

Next, a photoresist is applied on the upper electrode **17** at a thickness of 1.5 μm by spin-coating. Then, a photoreticle for fabricating the upper electrode is used to expose and develop the photoresist in order to form a resist pattern **18**. Subsequently, the resist pattern **18** is used as a mask to etch the upper electrode layer **17** (Figure 2F ~~3F~~). As etching conditions, for example, a high density plasma ICP etcher is used and the settings are as follows: Source power 2000 W; Bias power 500 W; Pressure 3 mTorr; Cl_2/Ar flow rate 30/90 sccm; and Etching depth 115 nm (15% overetching based on the thickness of the upper electrode with considering a thickness fluctuation 10% and a etching rate fluctuation 10%).

Please amend the paragraph extending from page 11, line 7, to page 11, line 13, as follows:

B26

After etching, an etching ~~depot~~ deposit **19** adhering to the pattern sidewall is removed by washing (e.g., by dipping into 10% concentration hydrochloric acid for 30 seconds). ~~and, then, the~~ The remaining resist pattern **18** is then removed by ashing (e.g., on

B26 amd.

a microwave down flow ashing apparatus: Microwave power 1000 W; Wafer temperature 250 C; O_2 flow rate 1000 sccm; Treatment time 3 minutes) (Figure 2G ~~3G~~).

Please amend the paragraph extending from page 11, line 14, to page 11, line 23, as follows:

B27

Next, a photoresist is applied at a thickness of 1.5 μm by spin-coating. Then, a reticle for fabricating the ferroelectric layer is used to expose and develop the photoresist in order to form a resist pattern **1a**. Subsequently, the resist pattern **1a** is used as a mask to etch the ferroelectric layer **14** (Figure 2H ~~3H~~). As etching conditions, for example, a high density plasma ICP etcher is used and the settings are as follows: Source power 2000 W; Bias power 500 W; Pressure 3 mTorr; Cl_2/Ar flow rate 30/90 sccm; and Etching depth 115 % based on the thickness of the remaining ferroelectric layer.

Please amend the paragraph extending from page 11, line 24, to page 12, line 5, as follows:

B28

After etching, an etching ~~depot~~ deposit **1b** adhering to the pattern sidewall is removed by washing (e.g., by dipping into 10% concentration hydrochloric acid 30 seconds). ~~and, then, the~~ The remaining resist pattern **1a** is then removed by ashing (e.g., on a microwave down flow ashing apparatus: Microwave power 1000 W; Wafer temperature 250 C; O_2 flow rate 1000 sccm; Treatment time 3 minutes) (Figure 2I ~~4I~~).

Please amend the paragraph extending from page 12, line 6, to page 12, line 16, as follows:

B25

Next, a photoresist is applied thereon at a thickness of 2.0 μm by spin-coating. Then, a photoreticle for fabricating the lower electrode is used to expose and develop the photoresist in order to form a resist pattern **1c**. Subsequently, the resist pattern **1c** is used as

a mask to etch the lower electrode layer **13** (Figure 2J ~~4J~~). As etching conditions, for example, a high density plasma ICP etcher is used and the settings are as follows: Source power 2000 W; Bias power 500 W; Pressure 3 mTorr; Cl_2/Ar flow rate 30/90 sccm; and Etching depth 230 nm (15% overetching based on the thickness of the upper electrode with considering a thickness fluctuation 10% and a etching rate fluctuation 10%).

Please amend the paragraph extending from page 12, line 17, to page 12, line 23, as follows:

After etching, an etching ~~depot~~ deposit **1d** adhering to the pattern sidewall is removed by washing (e.g., by dipping into 10% concentration hydrochloric acid 30 seconds). ~~and, then, the~~ The remaining resist pattern **1c** is then removed by ashing (e.g., on a microwave down flow ashing apparatus: Microwave power 1000 W; Wafer temperature 250 C; O_2 flow rate 1000 sccm; Treatment time 3 minutes) (Figure 2K ~~4K~~).

Please amend the paragraph extending from page 12, line 24, to page 13, line 2, as follows:

Finally, in order to recover electrical properties of the ferroelectric layer ~~from a damage~~ damaged ~~in the electrical properties caused~~ by etching, washing and ashing, an annealing operation is performed, for example, under a N_2 atmosphere at 650 °C for 30 minutes.

On page 13, between lines 5 and 6, please add the following new paragraphs:

Figure 2A - Figure 2J, previously described, illustrate a semiconductor device with a convex region provided on the upper surface of the ferroelectric layer. It has previously been mentioned that the upper surface of the ferroelectric layer can have a convex or

concave region. Accordingly, Figure 3 shows another embodiment in which the upper surface of the ferroelectric layer 14 has a concave region.

B32 cr c

Figure 4 shows a further embodiment in which a convex or concave region is also formed on the upper surface of the lower electrode. The convex or concave surface formed of the ferroelectric layer is thoroughly covered with the upper electric layer, and the convex or concave region formed on the upper surface of the lower electrode layer is thoroughly covered with the ferroelectric layer.